SEM-IV SE (ETRX) CBSGS 25/5/16

Microprocessor & Peripherals **Q.P. Code : 548001**

(3 Hours) **Total Marks:80**

N.B. 1) Question **number 1** is compulsory.
2) Attempt **any three** from remaining five questions.
3) Assume suitable data wherever necessary.
4) Figure to **the right** indicates full marks.

Q1. Attempt any four from the following (20)
a) At reset, interrupts in 8086 processor are disabled. Give reason.
b) List the differences between 8086 and 8088 processor.
c) Explain the feature of pipelining and queue in 8086 architecture.
d) Explain the significance of HOLD, RESET and READY signals in 8086 processor.
e) For 8086 op-code fetch machine cycle explain the significance of each T-state.

Q2)a) Classify and explain 8086 instruction set. (10)
b) Explain programmable interrupt controller 8259 – features and operation. (10)

Q3) a) Explain 8086-8087 coprocessor configuration in maximum mode of operation. (10)
b) Explain the following 8086 instructions
a) CMPSB b) DIV AX c) LOOPE again d) REP SCASB e) XLATB (10)

Q4) a) Write a detailed note on the interrupt structure of 8086 processor. (10)
b) Explain the need for DMA and modes of DMA data transfer. (10)

Q5) a) Explain the architecture of 8086 processor. What is the need for memory segmentation. (10)
b) With the help of a neat flowchart/algorithm write a program in 8086 assembly to arrange a set of ten 8-bit numbers initialized in data segment in ascending order. (10)

Q6) a) Write a brief note on programmable peripheral interface (PPI) IC – 8255 and its modes of operation. (10)
b) Using string instructions write a program in 8086 assembly to copy a block of ten bytes initialized in data segment to extra segment. Assume the necessary details. (10)
